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Exploration and Simulation of Network on Chip Topologies

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Abstract—*The network performance research and development have expanded in the recent years. A network on chip architecture gives a way to create a complex integrated circuit with an aim to deduct interconnections, facilitate simplicity and enhance network performance. This includes the design of topology which can directly affect the network performance by varying performance metrics like degree, diameter, and network cost. This works includes study, and simulation of various topologies and analysis on the basis of degree, diameter, network cost, simulation time, memory usage, and CPU usage.*

1. INTRODUCTION

A computer network embodies two or more computers which are associated in favor of trading data files, service and communication with making use of data link. The bonds within nodes are formed by a data link. Hardware and software are two particular of a computer network. Adapter, cable, router, and bridges which represents physical connection within machines are of hardware type. Whereas, the one which deals with rules and guideline of communication within machines is software. The pattern of setting nodes and data links in a network is termed as topology.[1] Depending upon the physical placement of cable and wires it is referred to physical topology. On the other hand, on the basis of fashion of binding of nodes and the way that the signs follow up on the system media, or the way that the information goes through the system starting with one machine onto the next it is stated as logical topology.[2] Separation of nodes, data flow rate, and physical interconnection can be different for a network even if topologies are equivalent. Network topologies are arranged into the accompanying essential sorts: Point-to-point, bus, star, ring, mesh, tree, hybrid and daiychain[3]. Topologies assume a noteworthy part in the region secured and network latency. In a network, routing is the procedure of selecting ways in a system along which drives the network activity and the route is the pathway to send the network movement. There are two ways routing takes place: static and dynamic. A static route is a course that is made physically by a system head which is physically arranged on the router [4]. Dynamic routing is a route learns by utilizing a routing protocol. For implementing this, a system-on-chip (SoC) design empowers the system topology to be reconfigured. The design hence empowers a summed up System-on-Chip (SoC) stage in which the topology can be redone for the application that is at present running on the chip [5].

The network on chip topologies was designed to optimize the network performance of the complete system thereby maintaining the various parameters like degree, diameter and network cost [6]. Along with this, the overall performance of the network is also affected by simulation time, memory utilized and fused CPU usage. This paper includes exploration of various topologies and analysis on the basis of this parameter. The lesser the simulation time, memory utilized, and CPU usage, the better the performance.

2. PERFORMANCE METRICS

The network performance can be evaluated by various parameters and these parameters determine the overall performance when data is transmitted within source and destination.

A. Degree

For a node, the degree is the number of connected links it has with other nodes. For determining the density of the network the average degree of the network is calculated. The cost of interfacing within a network is directly proportional to the degree of the network [7].

B. Diameter

Within a network, it is the smallest route for two far-flung nodes. But, when least route distance within all nodes is determined, diameter becomes the larger for all calculated routes. The diameter also shows the linear size of the network. This is used in determining the overall performance of the network. In some cases, diameter limits the lower limit for running an algorithm [8].

C. Network cost

The distance between two nods, a load of message congestion, error forbearance are based on diameter and degree of a network. Whereas, degree * diameter act as a touchstone for evaluating the association between network cost and potential for a multiprocessor system. When a network has high diameter value provides less message surpassing bandwidth and a network with more diameter value is very over-priced. Network cost also can be determined by the cost of routers, cable wires, and boards. And the cost of the link is being controlled by its distance, and place at pack configurations [9]. For a topological network, the cost can be determined by:

Network cost = Degree X Diameter

D. Memory utilized

For a network, memory utilized is the memory resources utilized when a message packet is sent between source and destination in a network. It is measured in KiloBytes(kb).

E. CPU Usage

It is the total CPU resources consumed when a message is transferred between source and destination within a network. It is measured in terms of Millisecond (ms).

3. NOC TOPOLOGIES

A. 3-D Mesh Network Topology

It is one of the basic elements of the network on chip topology. In this, all the links of a single node are in connection with its four closed adjoining nodes in order to complete communication.

Its architecture constitutes regular and uniform length links. It has many ways to reach from one node to another within architecture [10]. For, N=3 and n=64:

Its average latency is O(sqrt(N))

Degree: 6

Diameter: N((n^(1/N))-1)

Network Cost: 6 N((n^(1/N))-1)

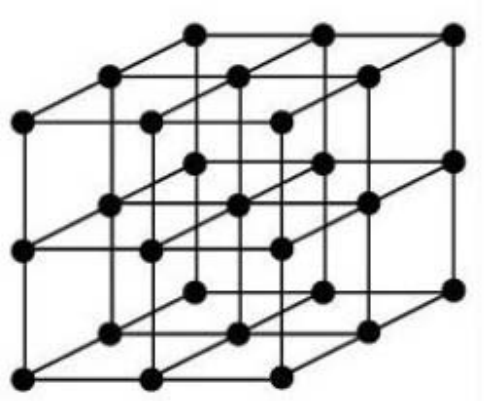

Fig. 1: 3-D Mesh structure

B. 3-D Torus

It is an extended version of 2-D Mesh architecture. It constitutes extra large loop edges inside two borderline nodes. But, when regularity is concerned, it has a higher-level architecture than Mesh, more uniform structure, the placement of the router and the inner plan. Torus architecture has an additional wrap around link which enhances diameter, network cost and thereby, affecting the overall performance of the network[11][12].

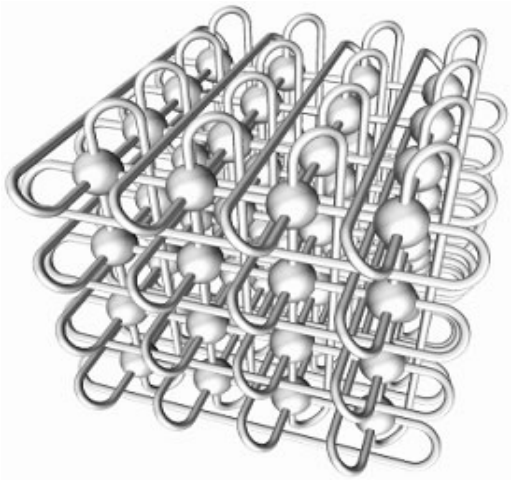

Fig. 2: Interconnection scheme within 3-D Torus topology

For, N=3 and n=64:

Degree: 6

Diameter: (N/2)(n^(1/N))

Network cost: 6 (N/2)(n^(1/N))

C. Hypertorus

For designing a hypertorus, a Torus is configured constituting a hypercube as a fundamental unit. The network designed by hypertorus has uniform node count and link length can be varied along with quality diameter.

The Cartesian product of hypertorus is formed by the graph of 3-Dimensional hypercube and torus. This Cartesian product evaluates the maximum productivity of hypertorus as it gives degree 4 which is lesser than the degree of its Cartesian products[13].

Degree: 4

Diameter: 0.35 sqrt(N)+4

Network cost: 1.4sqrt(N)+16

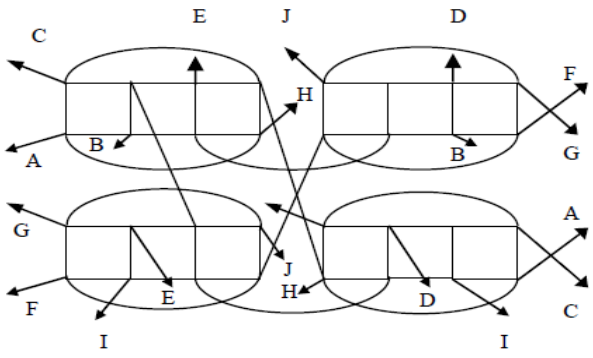

Fig. 3: Hyper-Torus QT (m,n)

4. SIMULATION COMPARISON AND TOPOLOGICAL ANALYSIS

Simulation is a process by which a simulator substantiates the functional accuracy of digital design which is modeled using hardware descriptive language (like Verilog). This process gives a response on the output pins of the circuit. Here, the simulation of the topologies has been done on Xilinx ISim 14.7 for Spartan 6. The comparisons of the studied architecture for N=3 and 64 number of nodes are as follows:

Table 1. Topological property comparison

Topology	Degree	Diameter	Network Cost
3-D Mesh	6	9	54
Torus	6	6	36
Hyper-Torus	4	7	28

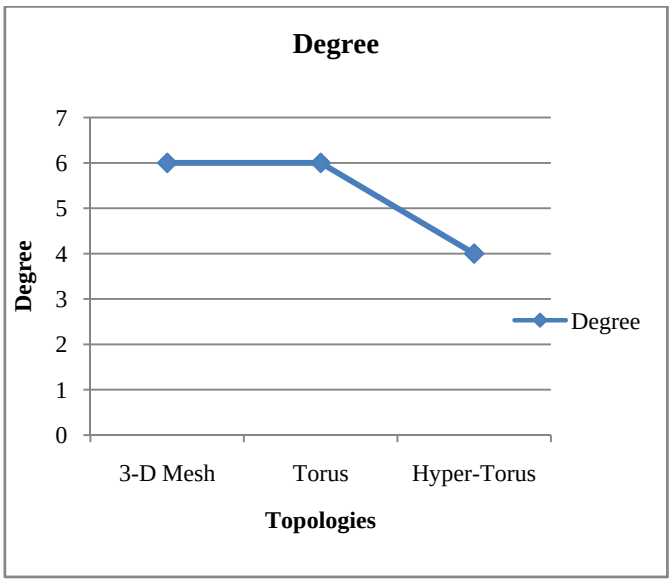

Fig.4. Comparison of degree for topologies

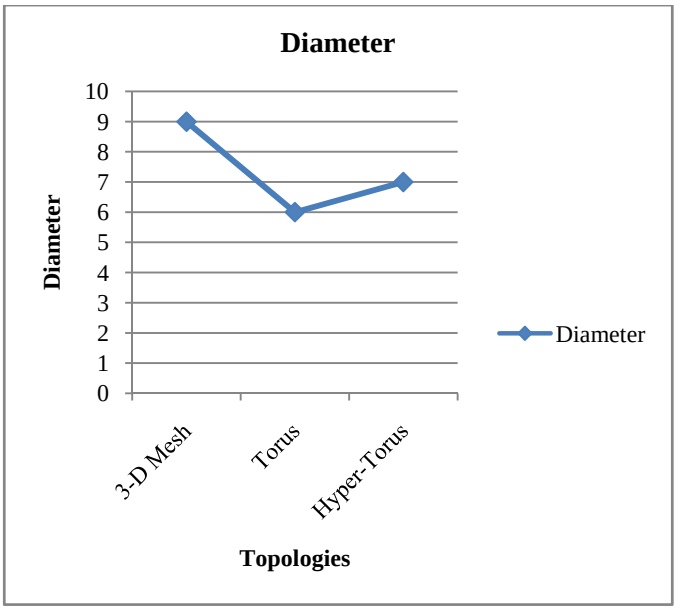

Fig.5. Comparison of Diameter for topologies

Table 2. Topological property comparison for Fuse memory and Fuse CPU usage

Topology	Fuse memory Usage (I)	Fuse CPU usage (I)
3-D Mesh	105964	312
Torus	105772	311
Hyper-Torus	105964	312

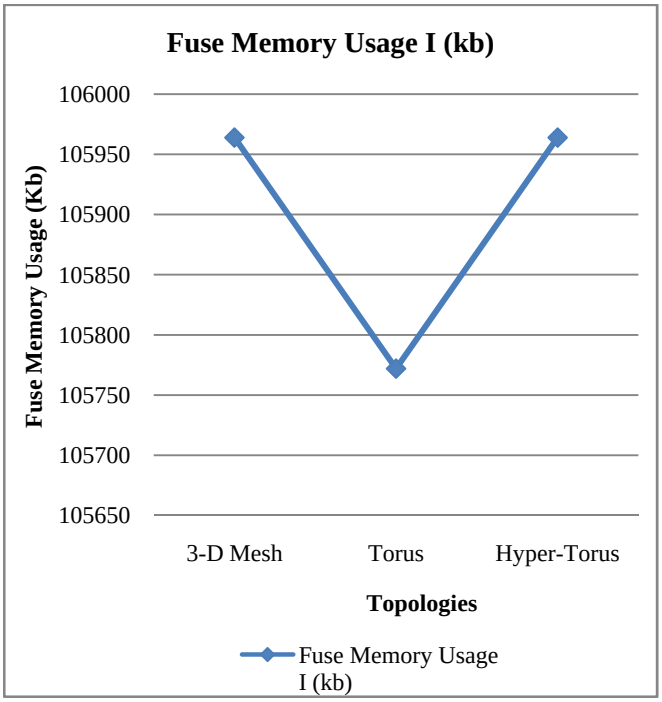

Fig.3. Comparison of Fuse memory usage(I) for topologies

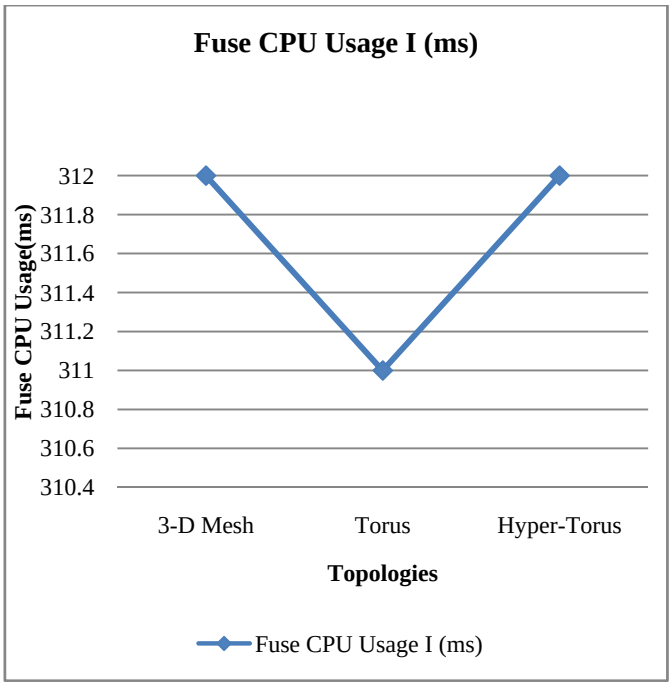

Fig.6. Comparison of Fuse CPU usage(I) for topologies

Table 3. Topological property comparison for Fuse memory and Fuse CPU usage

Topology	Fuse memory usage(II)	Fuse CPU usage(II)
3-D Mesh	110500	373
Torus	110350	342
Hyper-Torus	110550	420

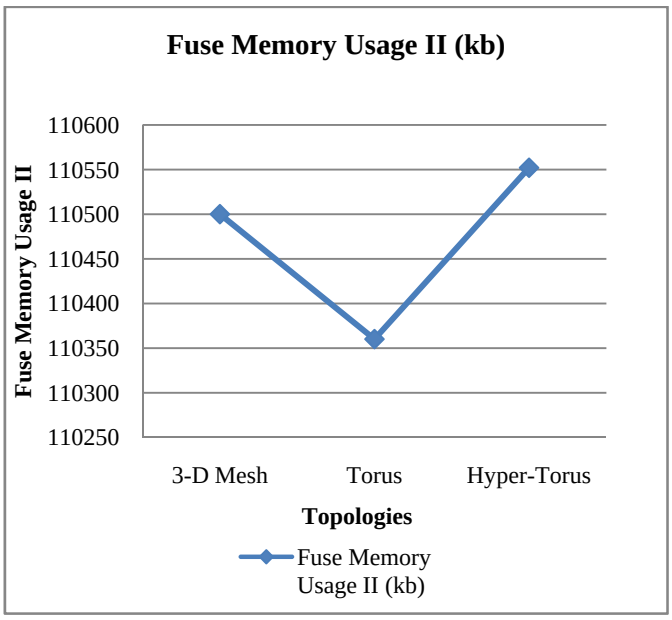

Fig.7. Comparison of Fuse memory usage(II) for topologies

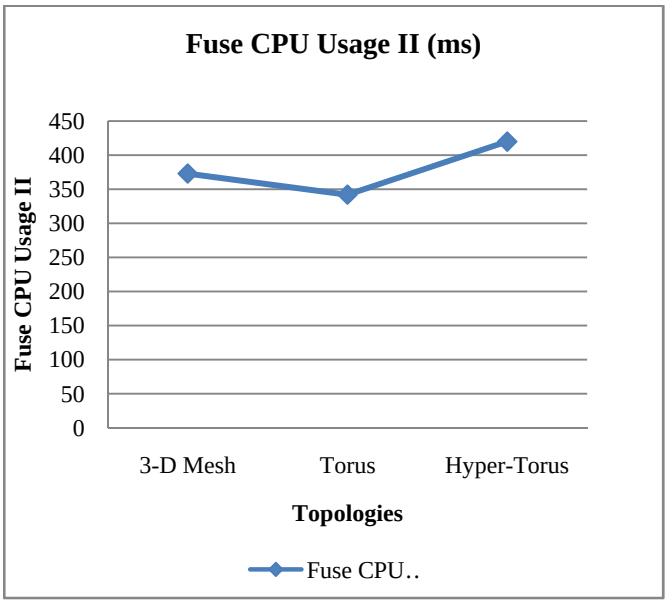

Fig.8. Comparison of Fuse CPU usage(II) for topologies

5. CONCLUSION

The simulation results corroborated that when the degree is compared Hyper-torus is better than 3-D Mesh and Torus. Torus has better diameter than 3-D Mesh and hyper-torus. But Hyper-Torus proves to have better network cost than the rest. Hence, making it the most suitable topology when it comes to contributing network performance as network cost is directly decreasing the cost of the network.

The simulation results revealed that Hypertorus takes more memory resources and CPU usage when it comes to simulation. But, Torus has taken least memory and CPU usage, making it most suitable topology when it comes to simulation. So, when network cost is considered, Hyper-torus is preferred, but for resource utilization, Torus is chosen.

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